



# Pulsar Boards and the Level II Trigger Upgrade at CDF

A presentation by Angela Little

SULI Program

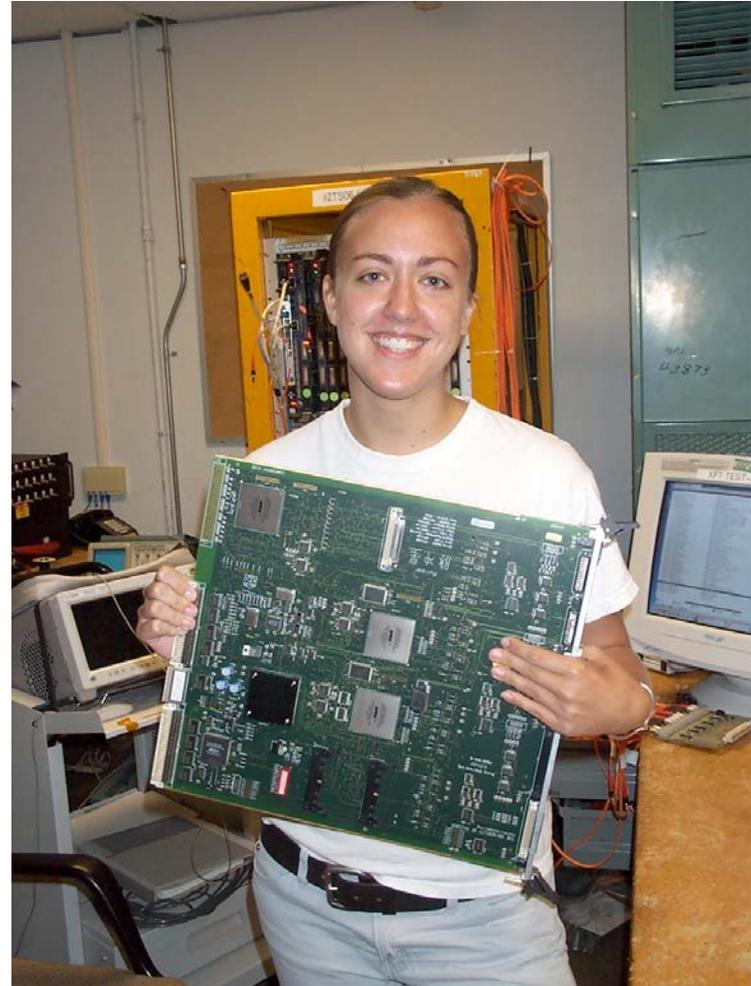
8/4/04

# Outline

- General Background
- Pulsar Boards
- Testing Pulsar Boards
- Testing Active Splitter
- Conclusions
- Acknowledgements

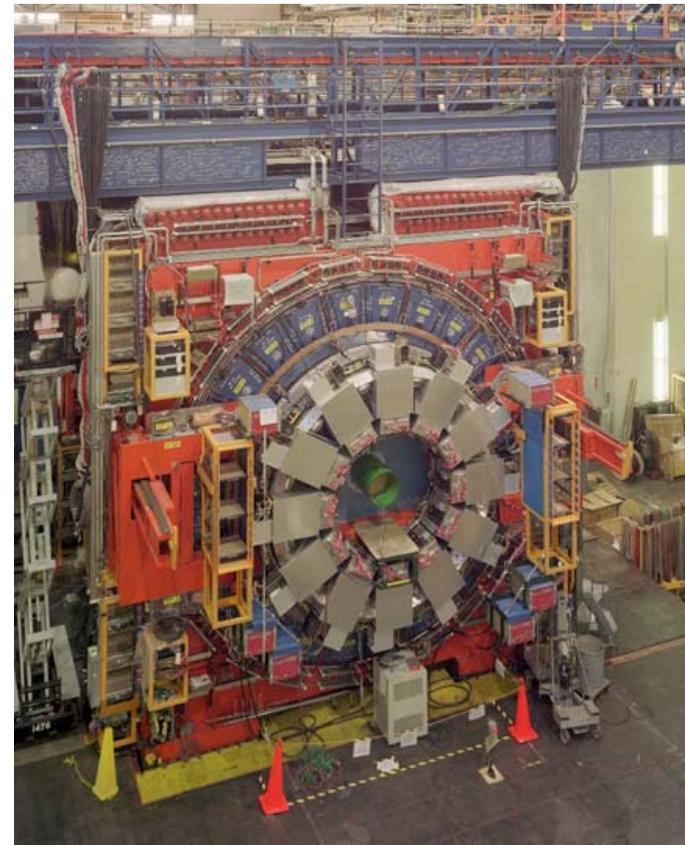
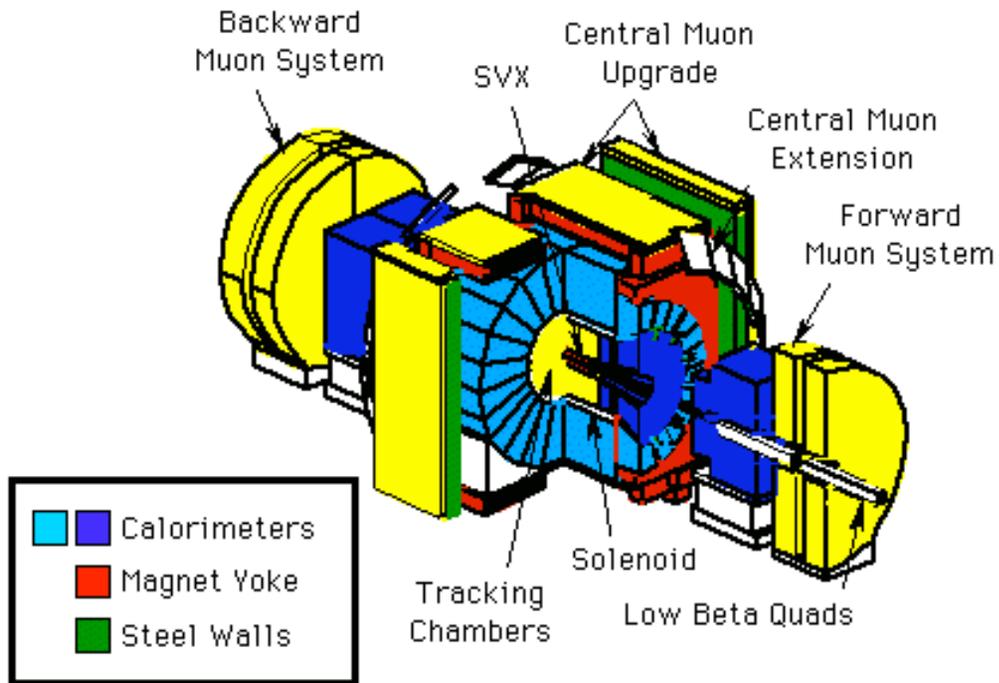
# My Summer Goals

- Test new Pulsar boards and mezzanine cards
- Document testing procedures
- Test active splitter
- Learn stuff

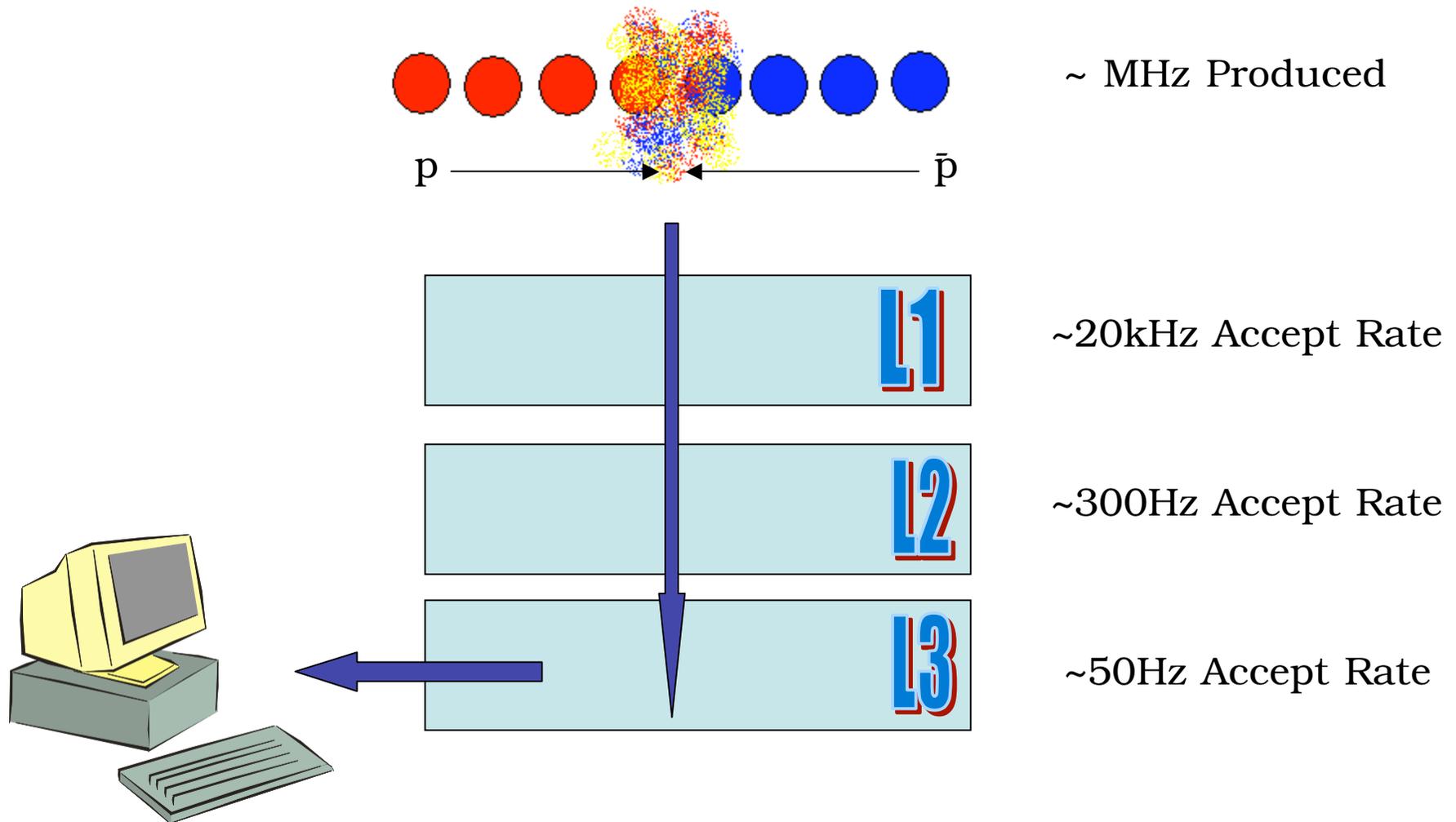


# CDF

## CDF Detector

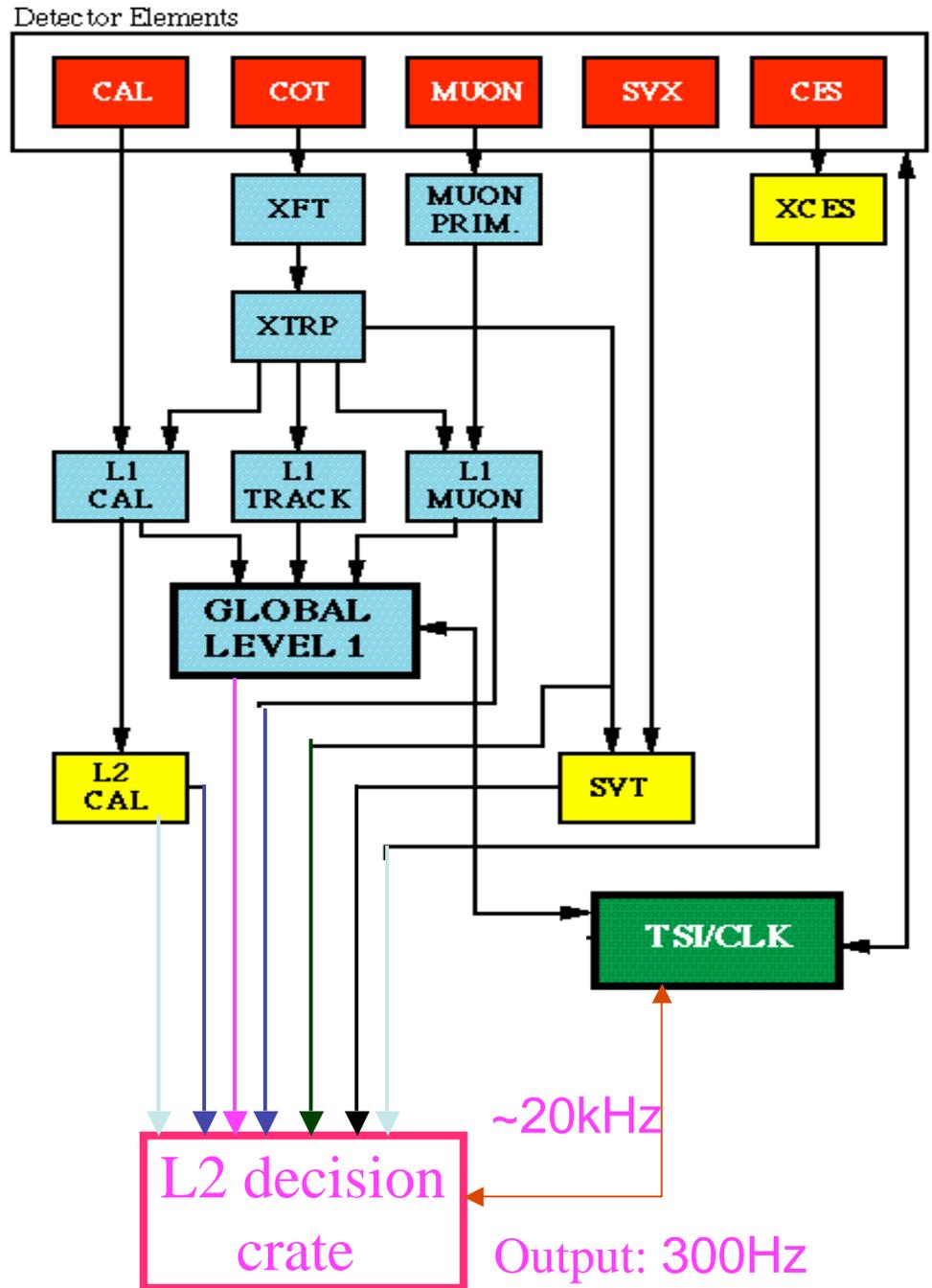
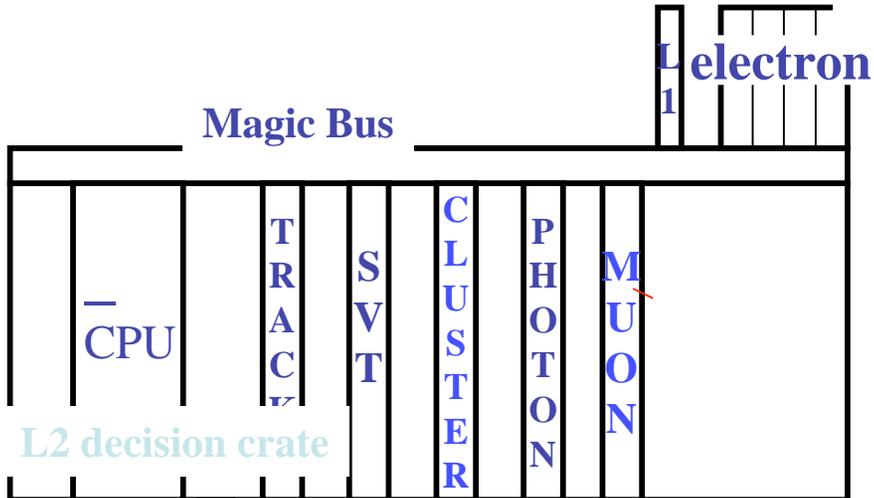


# Trigger: Filtering of Events



# Current L2 System

- Many Data Paths
- Custom Alpha Processor
- Custom Backplane
- Different Boards for Different Data Paths



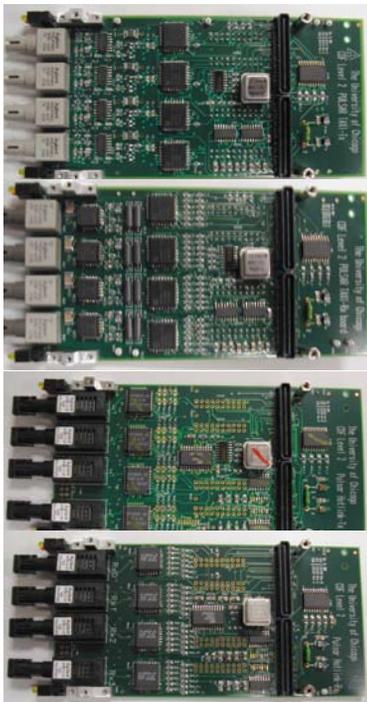
# L2 Upgrade

- Use one type of board to interface with ALL data paths
- Interface with modern CPUs, better performance
- More flexibility
- Fully self-testable, board & system level
  - crucial for commissioning & maintenance

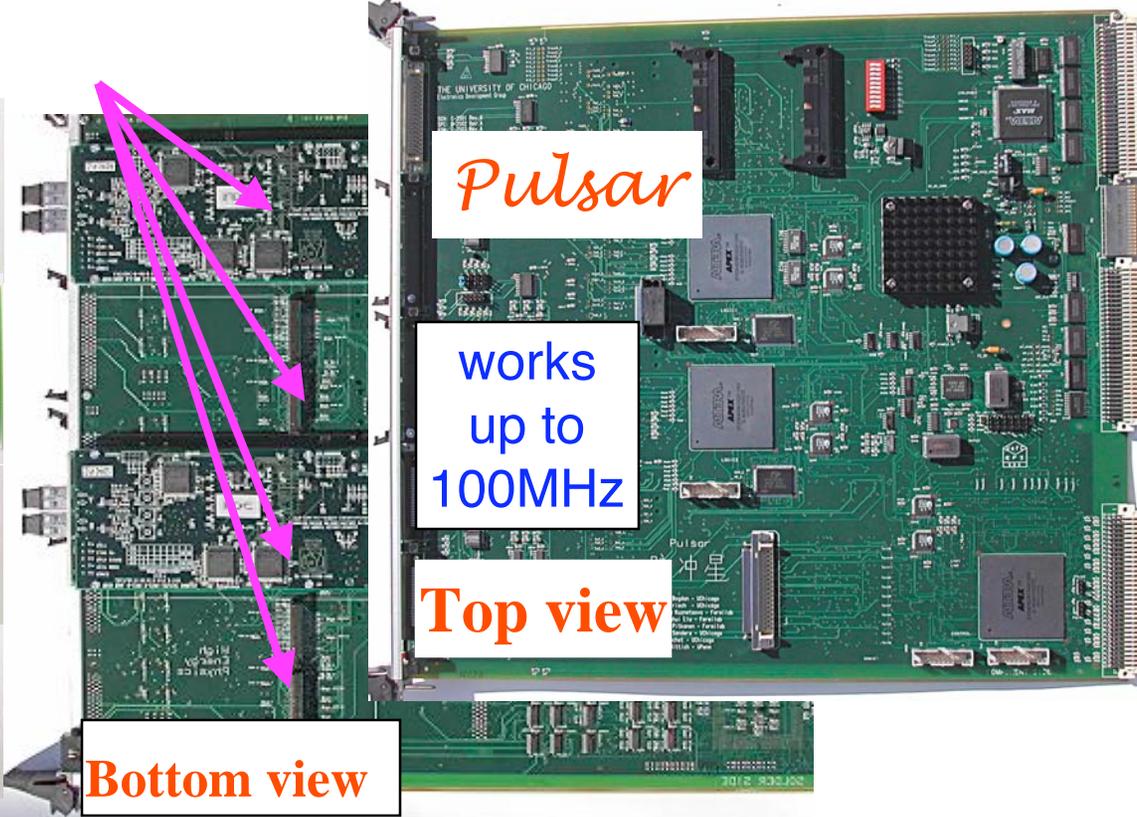
# Pulsar Design

→ universal/self-testable

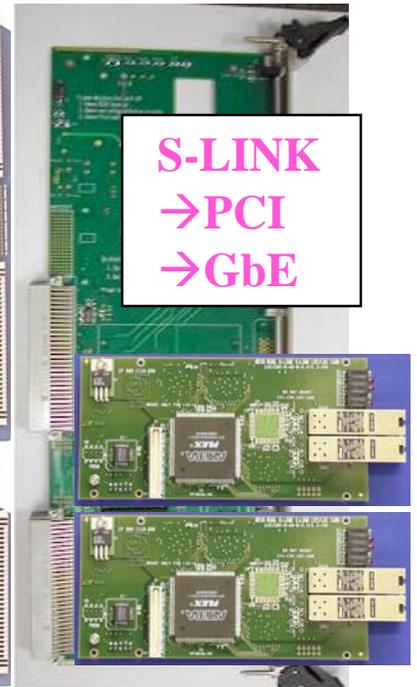
Custom mezzanine



Mezzanine slots



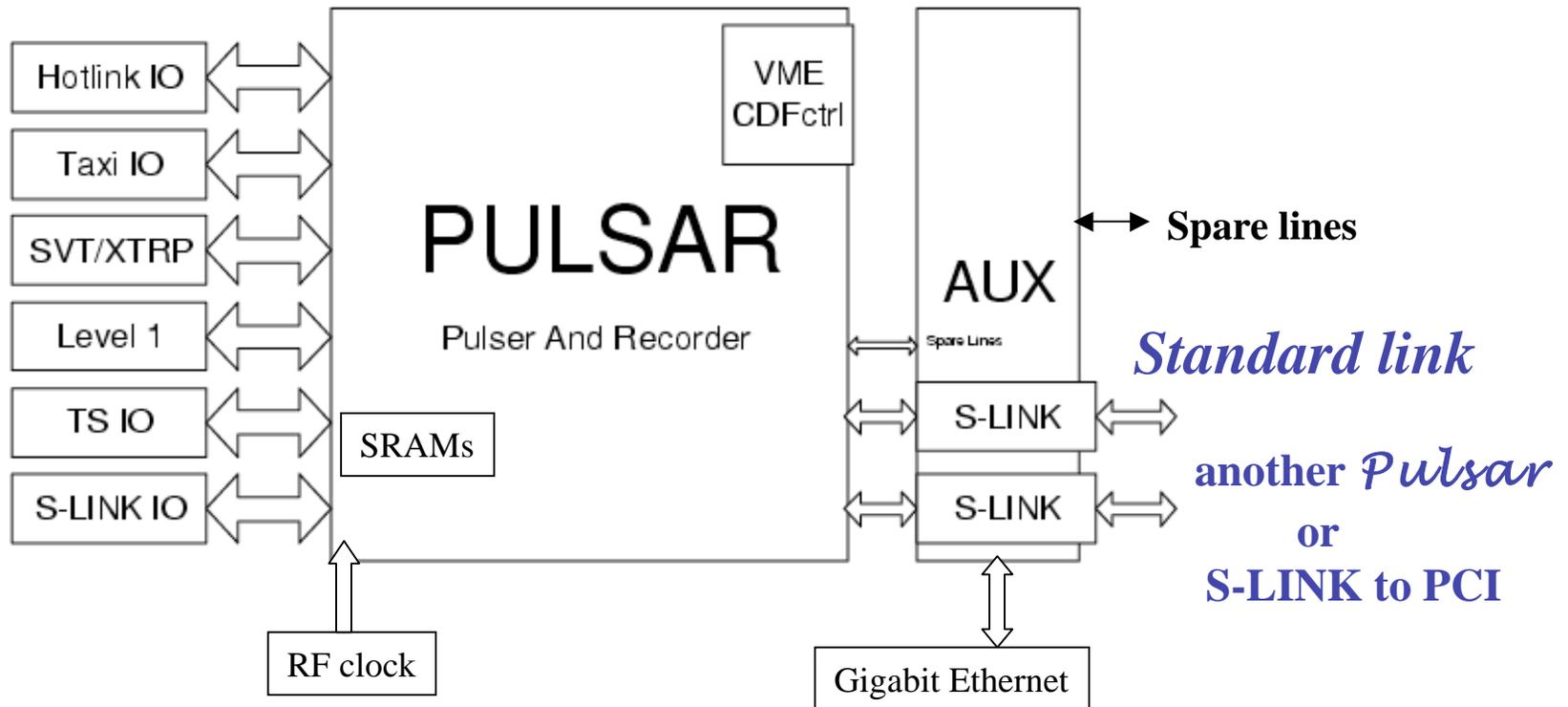
AUX card



*Pulsar design philosophy: able to interface with any user data with any link format (e.g. S-LINK) via mezzanine*  
*Many applications within & outside CDF (compatible with Atlas)*

# Pulsar board design

general purpose, can be used within/outside CDF



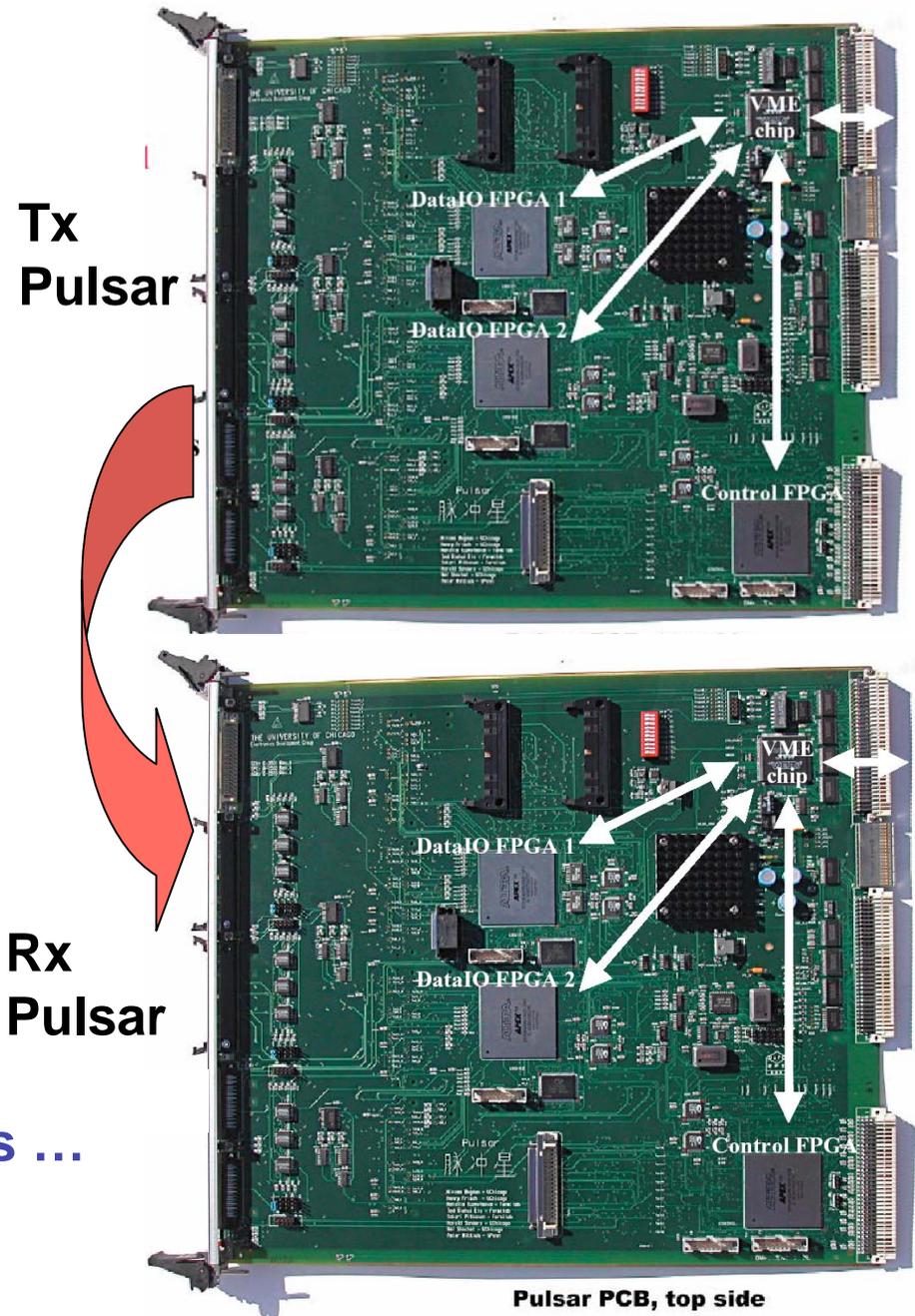
**All interfaces are bi-directional (Tx & Rx)  
→ self-testable**

# Testing ALL Interfaces on Pulsar

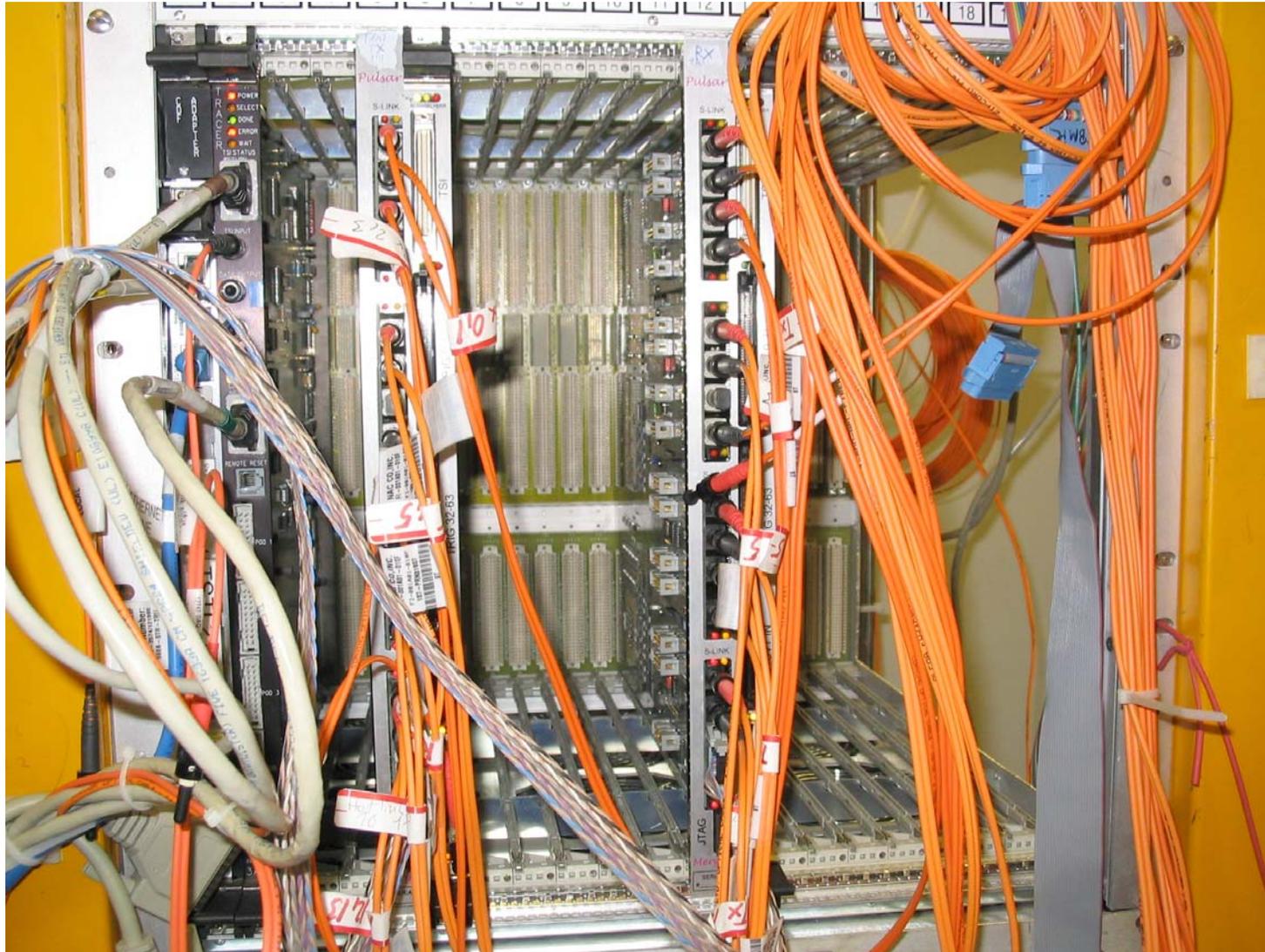
What needs to be tested:

- VME interfaces
- FPGA internal memory
- all LVDS interfaces
- all mezzanine card interfaces
- ...

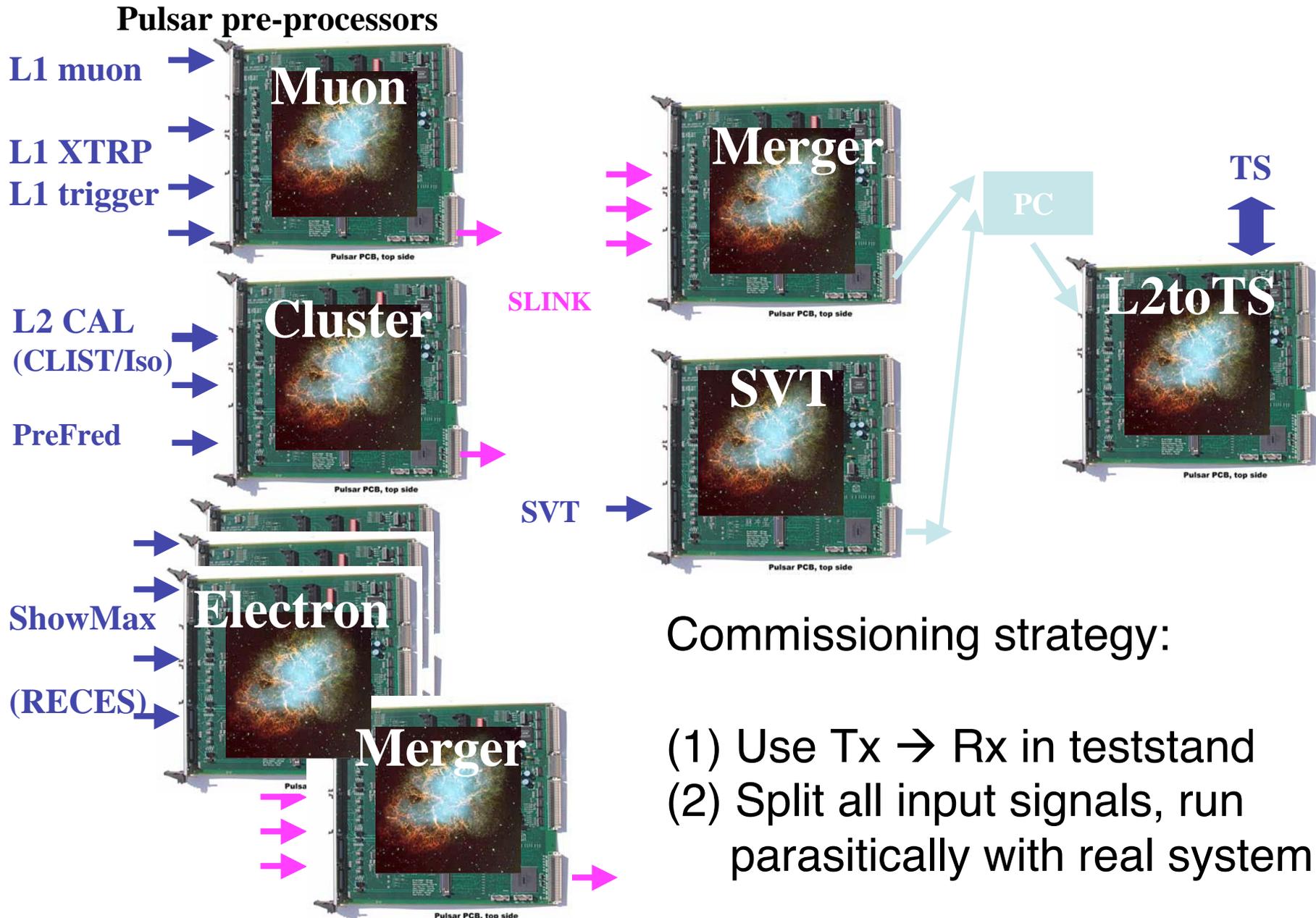
I have tested a few Pulsars this way, and am currently documenting the testing procedures ...



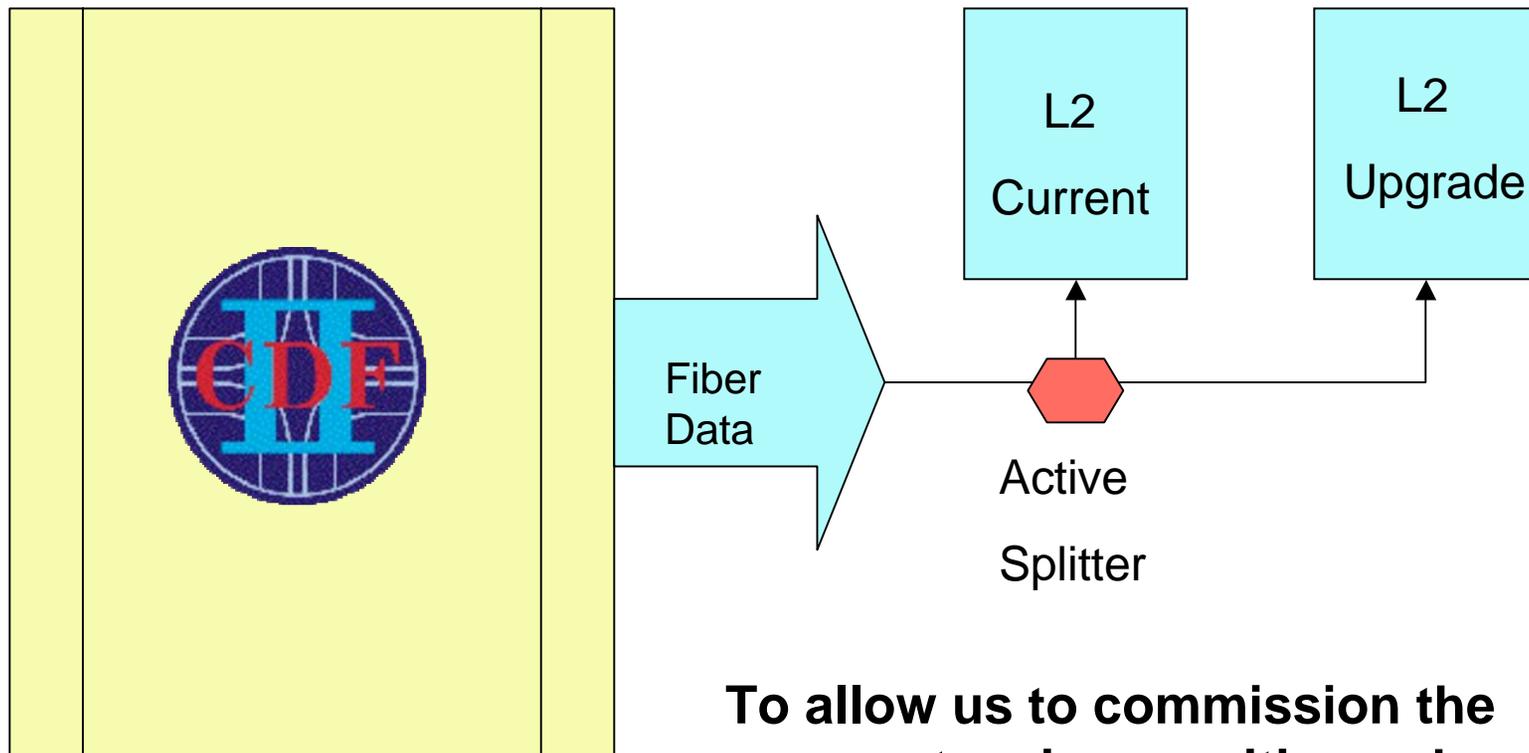
# Teststand Setup



# Pulsar based new L2 decision

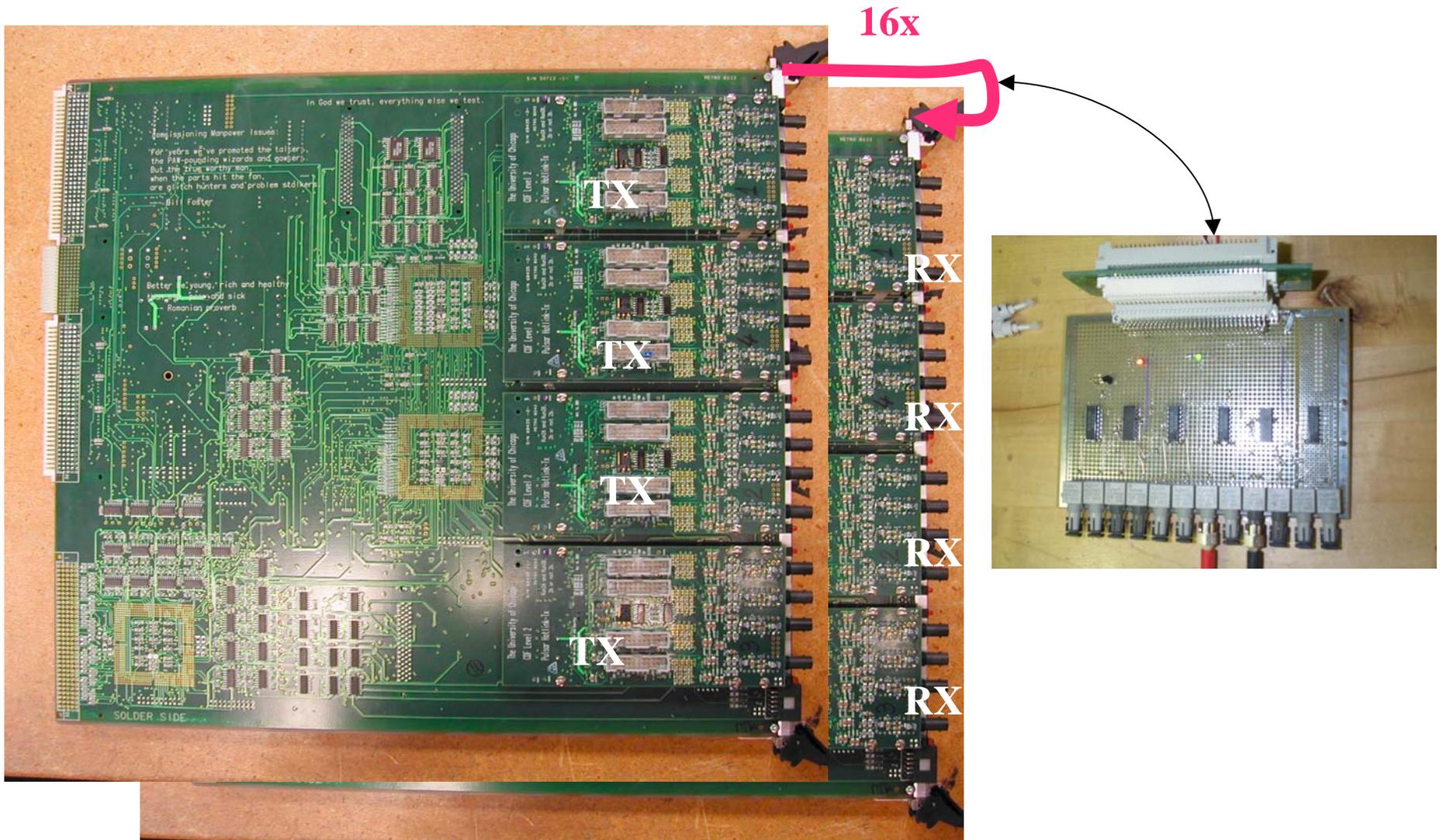


# Why do we need an Active Splitter?

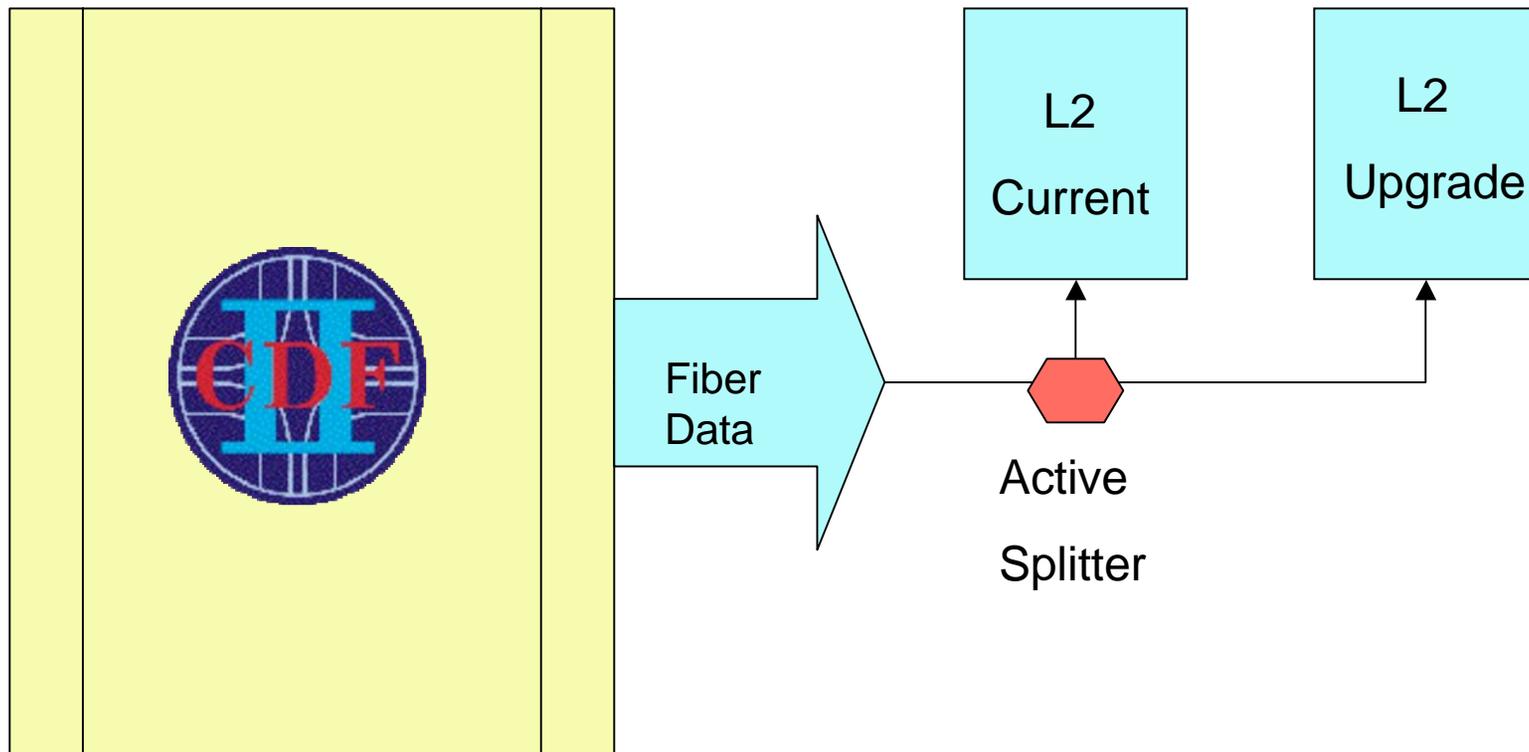


**To allow us to commission the new system in parasitic mode**

# Using Pulsar to Test the Active Splitters



# Goal



# Summary

- I have learned a lot, about CDF L2 trigger in general, and the Pulsar board in particular
- I have tested new Pulsar boards and documented the testing procedures
- I have helped to test active splitters which will be used to commission the new L2 system

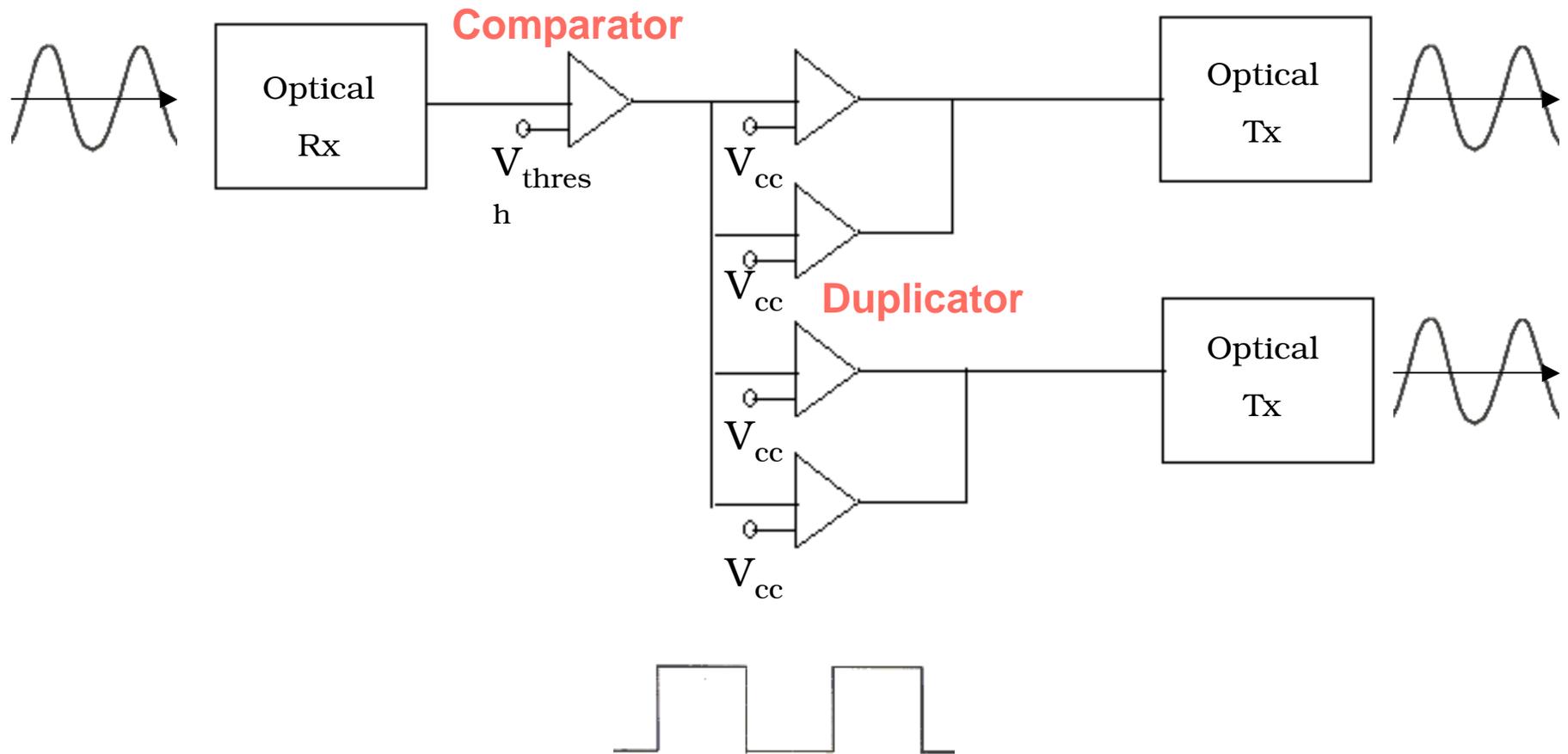
# Acknowledgements

- SULI Program and Fermilab
- Erik, Roger, and Max
- The Interns
- Ted Liu
- Burkard Reisert, Cheng-Ju Lin, and Chris Neu
- Pulsar Group

# Works Cited

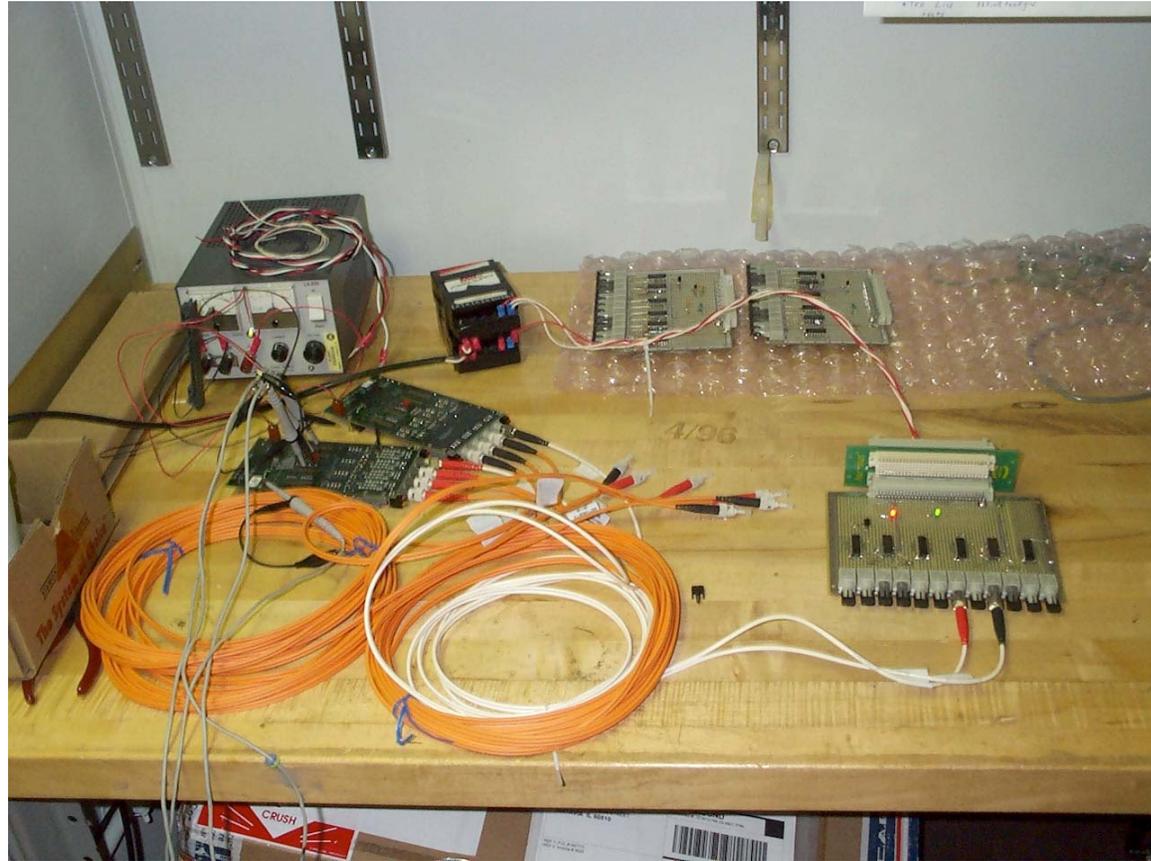
- *Pulsar Project*. University of Chicago/Fermilab.  
25 July 2004.  
<<http://hep.uchicago.edu/~thliu/projects/Pulsar/>>.

# Active Splitter Diagram

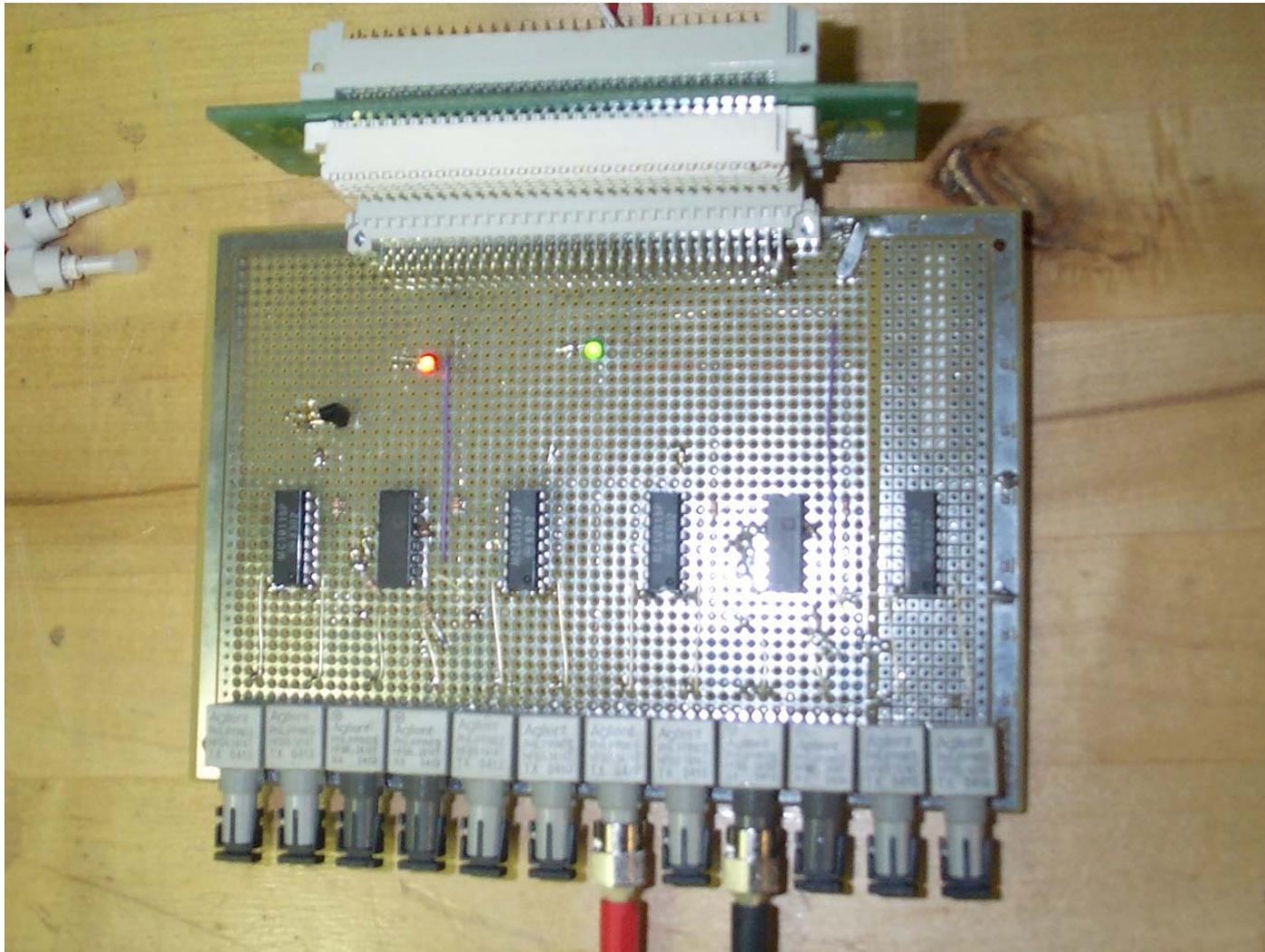


# Testing Active Splitter

- Testing

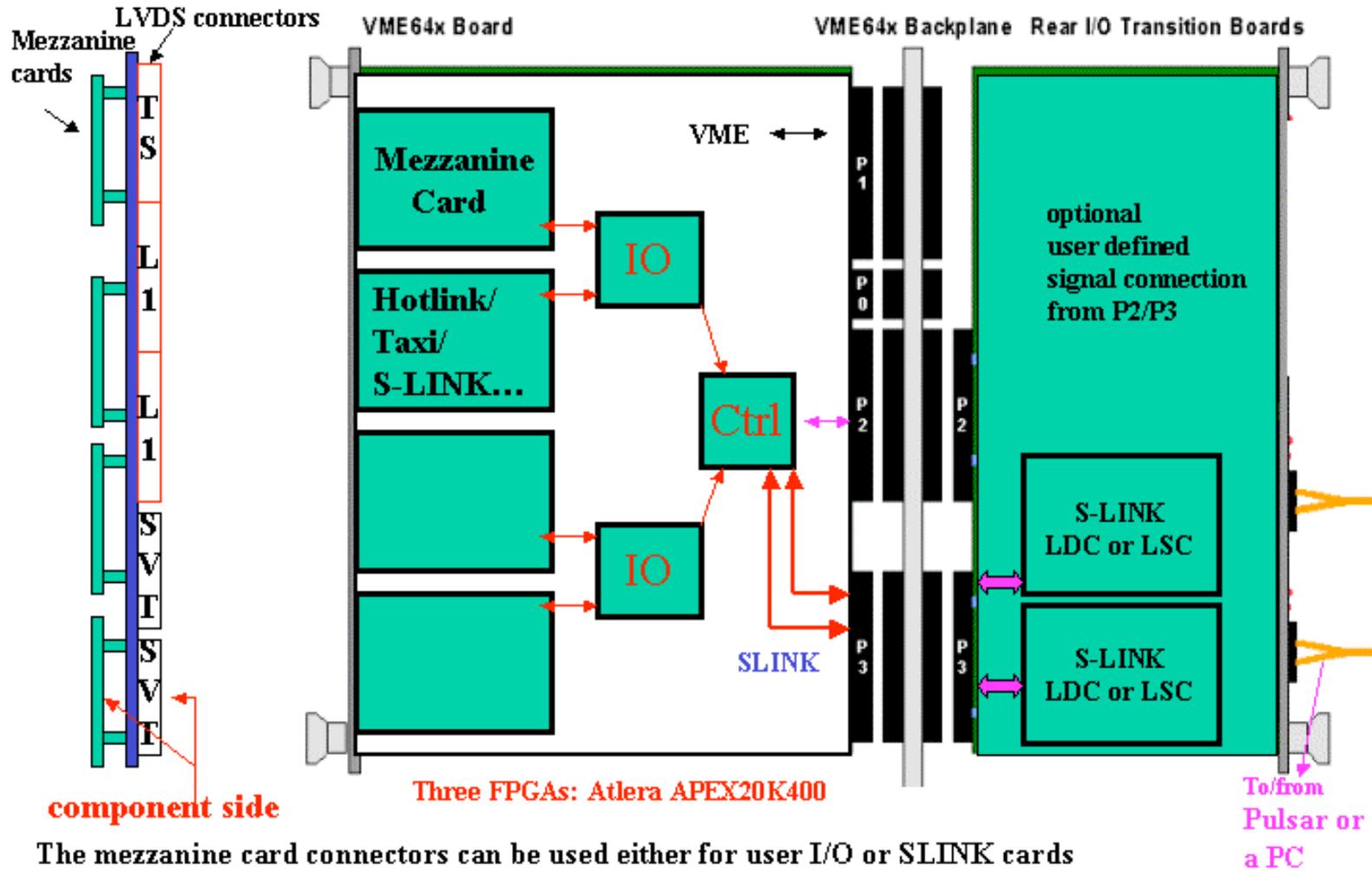


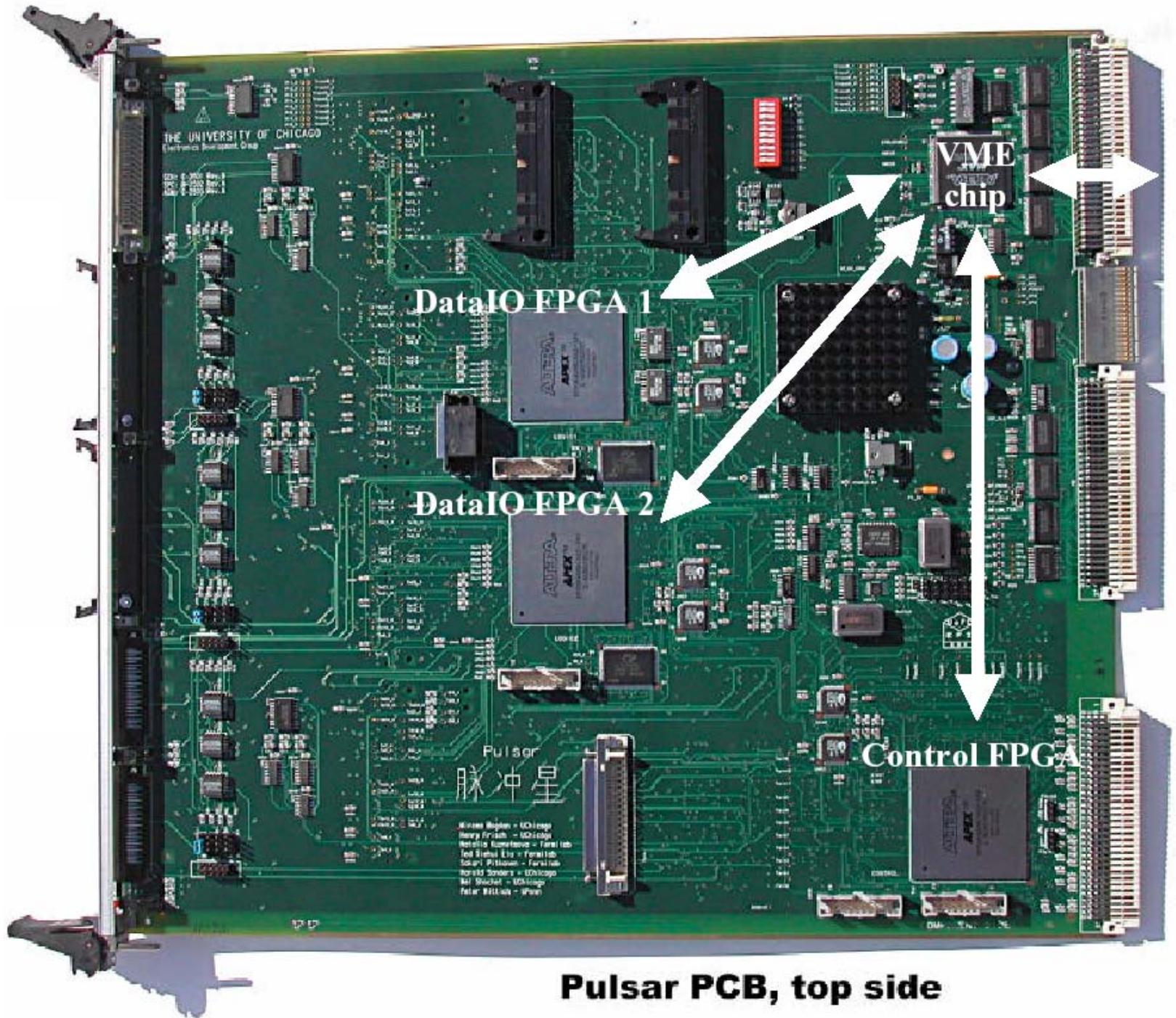
# The Active Splitter



Front-panel  
(double width)

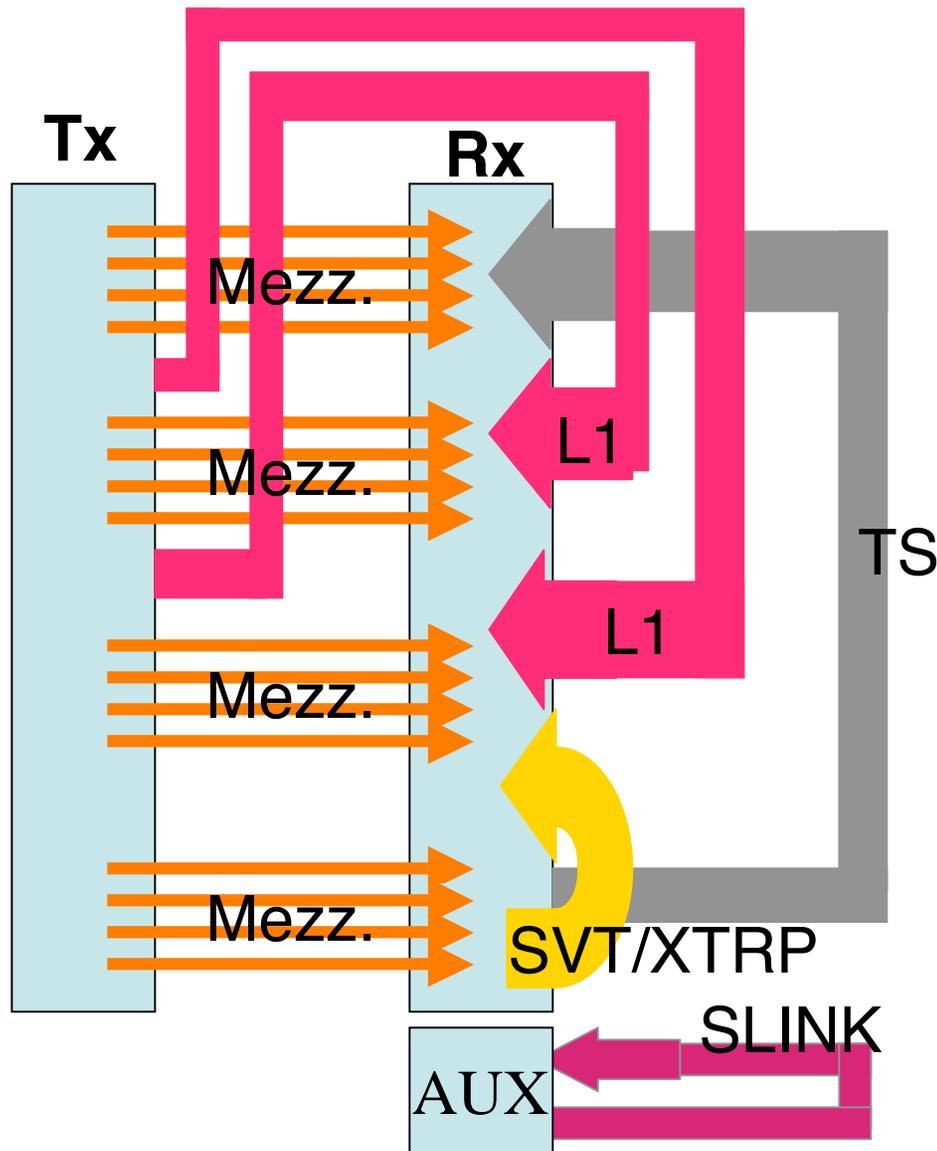
## PULSAR design





**Pulsar PCB, top side**

# Test Stand for Production Testing



- VME access
- Internal RAM and SRAM
- Internal com.
- TS interface
- SVT/XTRP
- L1 Signals
- Mezzanine card Interface
- Slink Interface